

<b>Notice of References Cited</b>	Application/Control No. 10/054,065	Applicant(s)/Patent Under Reexamination FRIEND ET AL.	
	Examiner Tan V Mai	Art Unit 2124	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,327,369	07-1994	Ashkenazi, Yaron	708/710
	B	US-6,373,290	04-2002	Forbes, Leonard	326/98
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Yee et al "Clock-Delayed Domino for Adder and Combinational Logic Design", 1996 IEEE, pp. 332-337.
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.